REMARKS

Claims 1-4, 6-15 and 17-20 remain in this application. Claims 1, 6, 7, 9 and 15 have been amended. Claims 5 and 16 have been cancelled. Claims 1, 9 and 15 are independent claims.

In the parent application, the Office action dated February 24, 2005 rejected claims 9-20 under 35 U.S.C. 102(e) as allegedly being anticipated by Takinosawa. Claims 1-8 were rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Takinosawa in view of Lesea. Applicant requests reconsideration of the claims in view of the amendments to claims 1, 6, 7, 9 and 15.

Claim 1 has been amended to incorporate the features of claim 5 as originally filed. In order to more particularly point out and distinctly claim the subject matter considered to be the invention, the test bus is identified in claim 1 as being dedicated to providing signaling for the enablement of detecting performance characteristics of individual SERDESs. Claims 6 and 7 have been amended to change their dependency from cancelled claim 5 to amended claim 1. Claim 9 has been amended in a manner similar to claim 1. Claim 15 has been amended to incorporate the features of claim 16 as originally filed.

A. Patentability of Independent Claim 9

In the parent application, claim 9 was rejected under 35 U.S.C. 102(e) as allegedly being anticipated by Takinosawa. Claim 9 describes an integrated circuit comprising a single semiconductor substrate onto which integrated circuitry is fabricated. A plurality of SERDESs are integrated onto the substrate, a plurality of functional test interfaces are integrally formed with the substrate, a plurality of functional test controllers are integrally formed with the substrate, an input/output controller and a common test bus are integrally formed with the substrate. The input/output controller is described as being connected to each FTC via a common test bus to transmit individually addressed commands to each FTC. In the Section 102 rejection of the claim, the teachings of Takinosawa are interpreted to teach a substrate having a single "functional test controller" 36 and a single "functional test interface" 35 for performing tests on a single SERDES. The rejection also interprets the USB Link Layer 12 as an input/output controller (IOC).

The USB Link Layer is depicted (Takinosawa: Fig. 1) as providing data (transmitting) a parallel format to USB Physical Layer 18 via data bus 21. In addition, USB Link Layer transmits content signals 23, which are identified as address commands to USB Physical Layer 18.

Referring to Fig. 2 of Takinosawa, data bus 21 is shown connected to the functional test controller 36. However, the TX controller signals 23, identified in the Office action as addressable commands, are shown connected to TX State Machine 41 (Takinosawa: Fig. 2). Therefore, USB Link Layer (IOC) transmits addressable commands to the TX State Machine not the functional test controller 36. In contrast, Applicant's amended claim 9 describes the IOC being connected to each FTC via a common test bus to transmit individually addressable commands to the FTC. Support for the amendment can be found in Paragraph [0021] of the application as originally filed, wherein each of the FTCs is connected to a common test bus 36, which may be used to transmit and receive data commands. Also connected to the test bus is an input/output controller (IOC) 38.

Referring again to Fig. 1 of Takinosawa, even if one were to form the USB interface 17 onto a single integrated circuit and the USB Link Layer was connected to a plurality of SERDESs and testers as taught by Takinosawa, the configuration of common test bus 21 and TX control signals 23 would not be analogous to an input/output controller connected to each FTC via a common test bus to transmit individually addressed commands to each FTC.

While Lesea was not cited in the Office action with respect to claim 9, Applicant submits that even if one were to modify the teachings of Takinosawa in view of Lesea, the resulting integrated circuit would not render claim 9 obvious under Section 103. In referring to Lesea on page 10 of the current Office action, Fig. 1 is cited for showing a plurality of SERDESs integrated onto a substrate. If one were to modify the teachings of Takinosawa to include multiple SERDESs onto a single substrate, the USB Link Layer would be connected to the TX State Machine of each SERDES to transmit addressable commands, and not connected to the functional test controller 36. Since the combination of teachings does not present a *prima facie* case of obviousness, Applicant asserts that claim 9 and its dependent claims are patentably distinguished from the teachings of Takinosawa and Lesea, whether taken separately or in combination.

Reconsideration of claim 9 and its dependent claims is requested.

B. Rejection of Independent Claim 15

Claim 15 has been amended to incorporate the features of claim 16 as originally filed in the parent application. Therefore, the patentability of amended claim 15 will be considered in view of the rejections of claims 15 and 16.

Claim 15 describes a method of testing operations of SERDESs of an integrated circuit, with the method including embedding a plurality of test interfaces and embedding a plurality of test controllers within the integrated circuit. The method also includes providing an integrated circuit output that enables the test controllers to be individually addressed and includes embedding an input/output controller (IOC) so that the IOC is connected between the integrated circuit output and the test bus to which each test controller is linked.

In rejecting claim 15, the Office action correctly pointed out that Takinosawa discloses that it is possible to conduct self test on two chips. The testing of two chips is described in paragraph [0048] on page 6 of the patent publication. Then, in the rejection of claim 16, it is stated that Takinosawa teaches that data to be transmitted is provided by the micro controller 12 to the "input/output controller" (i.e., the USB link layer 16). Since the USB link layer 16 is an integral part of the SERDES, duplication of the SERDES necessarily results in duplication of the "input/output controller." In claim 15, the method includes providing the integrated circuit output that enables test controllers to be individually addressed and includes connecting the input/output controller between this integrated circuit output and a test bus. Such connectivity is not described in Takinosawa, even if one were to duplicate the circuitry of Takinosawa as suggested in the Office action.

Fig. 1 of the pending application shows one possible implementation of the invention. In this implementation, the input/output controller 38 is connected between the test bus 36 and the integrated circuit output (SERIAL PORT). Because amended claim 15 describes each test controller being linked to the test bus and describes the input/output controller as being between the test bus and the integrated circuit output, the input/output controller cannot be an integral part of the SERDES. Therefore,

the USB link layer 16 of Takinosawa does not teach or suggest the input/output controller of amended claim 15.

While Lesea was not cited for teaching the obviousness of the combination of claims 15 and 16, Applicant respectfully points out that the connectivity resulting from the method described in amended claim 15 is not suggested in Lesea, even if combined with the features Takinosawa. It follows that the combination of prior art references does not present a *prima facie* case of obviousness with respect to the amended claim.

Reconsideration of claim 15 and its remaining dependent claims is requested.

C. Rejection of Independent Claim 1

Claim 1 has been amended to describe each tester as being connected to a common test bus and to describe each tester as having a unique address that enables independent accessibility of the tester via the test bus. The test bus is dedicated to providing signaling for the enablement of detecting performance characteristics of the individual SERDESs.

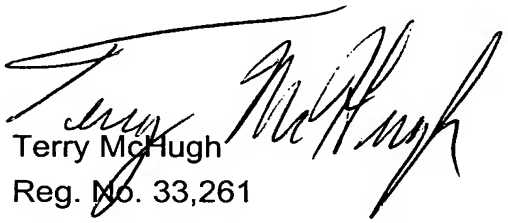
The amendment to claim 1 incorporates the features of claim 5 as originally filed. Specifically, the description of the test bus was incorporated from original claim 5. In the rejection of claim 5, the Office action states that Takinosawa teaches "the USB link layer 16 (core processing logic) functions to provide data to be transmitted in a parallel form (e.g., 16 bit word) to the USB physical layer 18 (SERDESs) via a data bus 21 (common test bus)." Unlike the rejections of independent claims 9 and 15, it is agreed that Takinosawa does not teach incorporating a plurality of SERDESs onto a single substrate. Page 2 of the Office action states:

> The Applicant rightfully relates the USB physical layer 18 comprises a built-in self-test (TX-BIST) circuit 35, a multiplexer 36 and a built-in self-analyzer circuit 49 to the tester circuit within the SERDES. However, it was not the Examiner's intention to identify these components as the "plurality of testers", but when the USB physical layer is repeated (i.e. the two USB physical layers on page 6, ¶ 48) it became a "plurality of testers". Since the built-in self-test (TX-BIST) circuit 35, multiplexer 36 and built-in self-analyzer circuit 49 is part of a single SERDES circuit or USB physical layer 18 it would stand to reason that these components comprise a single tester circuit.

Since Takinosawa does not teach a plurality of SERDESs or a plurality of testers on a single substrate, there is no teaching or suggestion that testers should be connected to a common test bus or that each of a plurality of testers should have a unique address that enables independent accessibility of the tester via the test bus. Lesea was not cited for teaching this feature. Moreover, amended claim 1 states that the test bus is dedicated to providing signaling for the enablement of detecting performance of characteristics of the individual SERDESs. A dedicated test bus is not taught or suggested by the cited prior art, even when combined as suggested in the Office action.

Applicant respectfully requests reconsideration of the claims in view of the amendments and remarks made herein. A notice of allowance is earnestly solicited. In the case that any issues regarding this application can be resolved expeditiously via a telephone conversation, Applicant invites the Examiner to call Terry McHugh at (650) 969-8458.

Respectfully submitted,



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